plate **134-2** has a second edge **208-2**, either or both of which may be customized shield plate edges having at least some portions that are non-parallel with d-sidewall **204** of gate electrode **130**.

[0046] As depicted in FIG. **5** and FIG. **6**, first edge **208-1** is displaced by a distance D**1** from d-sidewall **204** while second edge **208-2 2** is displaced by a distance D**2** from d-sidewall **204**. Although D**2** is greater than D**1** as shown in FIG. **6**, in other embodiments D**2** may be less than or equal to D**1**. In addition, because first and second edges **208-1** and **208-2** may both be customized shield plate edges, the relationship between D**1** and D**2** may vary over the extent of d-sidewall **204** such that D**1** may be greater than D**2** at some points, less than D**2** at other points, and equal to D**2** at still other points.

[0047] Both of the field plates **134-1** and **134-2** in FIG. **5** and FIG. **6** may be grounded or otherwise biased to a predetermined potential. The field plates may be biased to the same potential as each other or to different potentials. In still other embodiments employing multiple field plates, one or more of the field plates may be floating, i.e., not electrically connected to any other structure and not biased to any potential. The thickness and material of the shield ILDs **132-1** and **132-2** may be differentiated from each other to achieve desired electrical characteristics. Similarly, the thickness and material for the field plates **134-1** and **134-2** may be the same or different. In embodiments that use a silicide such as WSi for field plate **134-1**, as an example, field plate **134-2** may be comprised of a first metal material such as aluminum, copper, or another metal or alloy. As depicted in FIG. **5** and FIG. **6**, the shield plate edges **208-1** and **208-2** overlie NHV region **114**, but may extend further to overlie or partially overlie all of NHV **114** and all or portions of drain region **122**.

[0048] Although the invention is described herein with reference to specific embodiments, various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of the present invention. Any benefits, advantages, or solutions to problems that are described herein with regard to specific embodiments are not intended to be construed as a critical, required, or essential feature or element of any or all the claims.

[0049] Unless stated otherwise, terms such as "first" and "second" are used to arbitrarily distinguish between the elements such terms describe. Thus, these terms are not necessarily intended to indicate temporal or other prioritization of such elements.

1. A transistor, comprising:

a semiconductor substrate including a surface layer extending from an upper surface of the epitaxial layer to a surface depth;

a gate dielectric overlying a channel region of the surface layer;

a gate electrode overlying the gate dielectric, the gate electrode including a first sidewall and a second sidewall;

a channel region comprising a portion of the surface region underlying the gate electrode;

a source region comprising a portion of the surface region extending between the channel region and a source contact region;

a drift region comprising a portion of the surface region extending between the channel region and a drain region;

a shield interlevel dielectric (ILD) overlying at least a portion of an upper surface of the gate electrode, the second sidewall, and a portion the drift region;

a shield plate comprising an electrically conductive layer overlying at least a portion of the shield ILD, the shield plate defining a shield plate edge overlying the drift region, wherein the shield plate edge comprises a customized shield plate edge wherein a displacement between the customized shield plate edge and the second sidewall varies along a length of the second sidewall.

2. The transistor of claim **1**, wherein the shield plate comprises a first shield, the shield plate edge comprises a first shield plate edge, and the shield ILD comprises a first shield ILD and wherein the transistor includes:

a second shield ILD including a portion overlying at least a portion of the upper surface of the gate electrode, the second sidewall, and a portion the drift region; and

a second shield plate comprising an electrically conductive layer overlying at least a portion of the second shield ILD, the second shield plate defining a second shield plate edge overlying a second shield ILD.

3. The transistor of claim **2**, wherein the second shield plate edge defines a second customized shield plate edge overlying the drift region, wherein a displacement between the second shield plate edge and the second sidewall varies along a length of the second sidewall.

4. The transistor of claim **2**, wherein the second shield plate defines a parallel shield plate edge wherein a displacement between the second shield plate edge and the second sidewall remains substantially constant along a length of the second sidewall.

5. The transistor of claim **4**, wherein the second shield plate overlies the first shield plate.

6. The transistor of claim **5**, wherein the first shield plate overlies the second shield plate.

7. The transistor of claim **2**, wherein the second shield plate overlies the first shield plate.

8. The transistor of claim **7**, wherein the displacement between the first shield plate edge and the second sidewall exceeds a displacement between the second shield plate edge and the second sidewall along a first portion of the first shield plate edge and wherein the displacement between the first shield plate edge and the second sidewall is less than a displacement between the second shield plate edge and the second sidewall along a second portion of the first shield plate edge.

9. The transistor of claim **2**, wherein a thickness of the first shield plate ILD differs from a thickness of the second shield plate ILD.

10. The transistor of claim **2**, wherein a thickness of the first shield plate differs from a thickness of the second shield plate.

11. The transistor of claim **2**, wherein the first shield plate is comprised of a first shield plate material and the second shield plate comprises a second shield plate material, wherein the first shield plate material differs from a second shield plate material.

12. The transistor of claim **1**, wherein the shield plate is comprised of a silicide.

13. The transistor of claim **1**, wherein shield plate edge comprises a plurality of line segments.